

REMARKS

Reconsideration and allowance of the subject application are respectfully requested.

Applicant notes with appreciation the Examiner's allowance of claims 1-15, 21, 23, and 24, as well as the indication of allowable subject matter in claims 19, 20, 32 and 33.

Claims 16-18, 25, 27-31 and 34-36 stand rejected based on newly-formulated prior art rejections. Each of these is addressed in turn.

Claims 25, 30, 31 and 35 stand rejected under 35 U.S.C. §102(b) as being anticipated by previously-cited and applied, U.S. Patent 5,694,419 to Lawrence et al. This rejection is respectfully traversed.

Lawrence does not teach every feature of claim 25 as required to satisfy the rigorous standards of anticipation. The Examiner relies on the VSB demodulator shown in Figure 5, and the descriptive text at column 9, lines 16-28. In Figure 5, only one of the real and imaginary inputs, i.e., the real input "I", is equalized. The equalized I component is used to perform timing recovery in block 580. In contrast, claim 25 recites that "one of the real and imaginary components of the known signal *which has not been equalized*" is used to control the timing unit. Here, Lawrence's *equalized* output is clearly controlling the timing unit 580. As stated at column 9, lines 17-18, "these *equalized* in-phase symbols are also applied to circuit 580 which recovers timing information therefrom." (emphasis added).

Lawrence also fails to disclose that "the other of the first and second mechanisms is arranged to (a) permit simultaneous equalization of the other of the real and imaginary components of the known signal by the equalizer, and (b) adapt the equalizer using only the other of the real and imaginary components of the known signal." The very same equalizer output "I" which controls timing recovery unit 580 is used to formulate the error signal generated by slicer 570 and feedback to adapt the equalizer 560.

Lacking multiple features recited by claim 25, the anticipation argument is improper and should be withdrawn. Applicant also traverses the anticipation rejection of dependent claim 31. Lawrence fails to disclose that "the first and second mechanism are arranged so that the equalizer is updated in a radial direction."

Claim 28 stands rejected under 35 U.S.C. §103 as being unpatentable over Lawrence, in view of U.S. Patent 6,088,401. This rejection is respectfully traversed.

First, Sato fails to remedy the deficiencies of Lawrence with respect to claim 25. Moreover, claim 28 recites that "the real component of the known signal is not equalized and the imaginary part of the known signal is equalized." In Sato's Figure 1, both the real (I) and imaginary (Q) signal components are equalized. The real component output from the synchronous detector 25 is equalized in the equalizer 9, and the imaginary component output by the synchronous detector 6 is equalized by the equalizer 10. Thus, the Examiner's interpretation of Sato is in error. The Examiner also fails to provide any reasonable motivation as to combine Lawrence with Sato. Why would Sato's teachings incorporated in Lawrence improve signal detection?

Claim 27 stands rejected under 35 U.S.C. §103 as being unpatentable over Lawrence in view of U.S. Patent 6,643,321 to Genossar. Genossar fails to remedy the deficiencies of Lawrence with respect to independent claim 25.

Claim 29 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Lawrence in view of U.S. Patent 6,496,229 to Limberg. Limberg fails to remedy the deficiencies of Lawrence with respect to claim 25. In addition, the Examiner's stated rejections for claims 34 and 36, even if assumed to be accurate for purposes of argument only, fail to remedy Lawrence's deficiencies with respect to independent claim 25.

Claims 16 and 18 stand rejected under 35 U.S.C. §103 as being unpatentable over U.S. Patent 6,573,293 to Scarpa et al. in view of U.S. Patent 6,088,401 to Saito. This rejection is respectfully traversed.

Scarpa discloses a QAM and VSB demodulator that can demodulate QAM or VSB modulated signals. The Examiner relies on Figure 2, which shows a VSB demodulator 200 that includes an equalizer 252, a slicer 256, and a timing recovery circuit 240. The "I" and "Q" components generated by the Hilbert transform filter 224 are both provided to an equalizer 252. The real component is also provided to the timing recovery circuit 240.

The Examiner admits that Scarpa fails to teach that "the equalizer only samples the imaginary component of the sample signal not the real component." The Examiner relies upon Saito, which as explained above, describes using two equalizers 9 and 10, to equalize *both* the real and imaginary components of a sampled signal—contrary to the

contention made by the Examiner. Thus, even if the combination of Scarpa and Saito could be made, for purposes of argument only, that combination fails to disclose all of the features recited in independent claim 16.


Moreover, the Examiner provides no substantive motivation for combining the teachings of Saito and Scarpa. The Examiner simply states that such combination would improve signal detection, without explaining how or why this is the case. In any obviousness analysis, it must be shown that there was a motivation or suggestion in the prior art to make the combination or modification. See for example *In re Rouffet*, 149 F.3d 1350, 1357-58 (Fed. Cir. 1998). A proper motivation to combine requires an appreciation of the *desirability* of making the combination. It is not measured by the *feasibility* of making the combination. See *Winner Int'l Royalty Corp. v. Wang*, 202 F.3d 1340, 1349 (Fed. Cir. 2000). The Examiner fails to show where such desirability for this combination is found in the prior art or elsewhere.

Applicant submits that the present application is in condition for allowance. An early notice to that effect is earnestly solicited.

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Respectfully submitted,

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